(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
16 May 2002 (16.05.2002)

PCT

(10) International Publication Number
WO 02/039290 A3

(51) International Patent Classification[7]: G06F 13/42

(21) International Application Number: PCT/US01/31816

(22) International Filing Date: 12 October 2001 (12.10.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/708,221 7 November 2000 (07.11.2000) US

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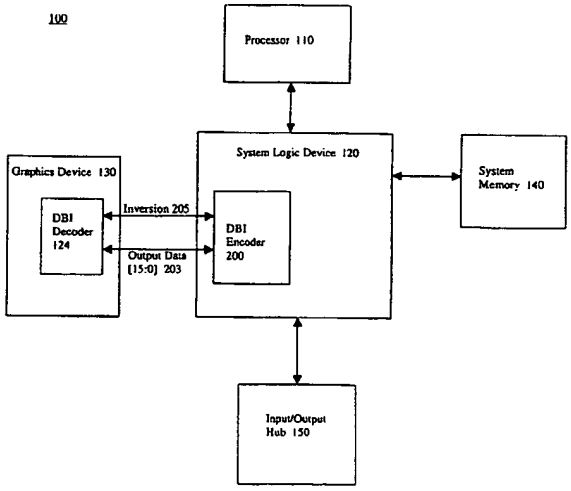
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

[Continued on next page]

(54) Title: METHOD AND APPARATUS FOR REDUCING SIMULTANEOUS SWITCHING OUTPUT NOISE USING DYNAMIC BUS INVERSION



(57) Abstract: An embodiment of a computer system implementing dynamic bus inversion includes a first system logic device having a dynamic bus inversion encoder and also includes a second system logic device having a dynamic bus inversion decoder. The first and second system logic devices are coupled via a data bus. The encoder compares a group of data bits currently placed on the data bus with a next group of data bits to be placed on the data bus. If the encoder determines that greater than a predetermined number of bit transitions would occur between the current and next group of data bits, the encoder inverts the next group of data bits before placing the next group of data bits onto the data bus. The encoder also asserts an inversion signal that is received by the decoder. In response to the assertion of the inversion signal, the decoder inverts the previously inverted next group of data bits to restore the original data.

WO 02/039290 A3

(88) Date of publication of the international search report:
3 April 2003

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/31816

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F13/42

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
PAJ, EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 1997, no. 07, 31 July 1997 (1997-07-31) & JP 09 069075 A (NIPPON TELEGR &TELEPH CORP <NTT>), 11 March 1997 (1997-03-11)	24,25
Y	abstract; figure 1	1-3,9-17
Y	US 5 960 468 A (PALUCH EDWARD J) 28 September 1999 (1999-09-28)	1-3,9-17
A	the whole document	4-8, 18-25
A	EP 0 520 650 A (AMERICAN TELEPHONE & TELEGRAPH) 30 December 1992 (1992-12-30) column 1, line 56 -column 2, line 19 column 3, line 60 -column 5, line 7 abstract	1-25

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 December 2002	19/12/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax (+31–70) 340–3016	Nguyen Xuan Hiep, C

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 01/31816

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 09069075 A	11-03-1997	NONE	
US 5960468 A	28-09-1999	US 6457114 B1	24-09-2002
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		JP 5210601 A	20-08-1993

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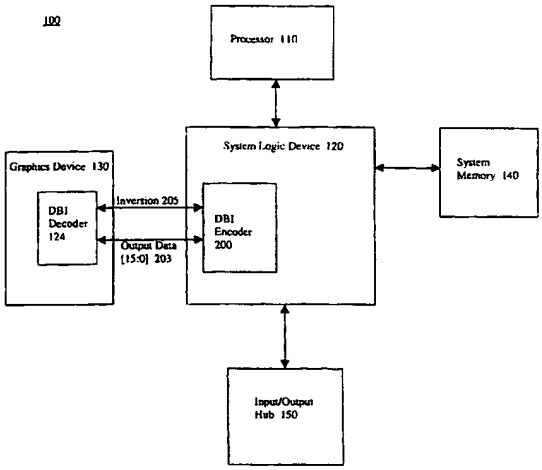
Published:
— *without international search report and to be republished upon receipt of that report*

[Continued on next page]

(54) Title: METHOD AND APPARATUS FOR REDUCING SIMULTANEOUS SWITCHING OUTPUT NOISE USING DYNAMIC BUS INVERSION



(57) Abstract: An embodiment of a computer system implementing dynamic bus inversion includes a first system logic device having a dynamic bus inversion encoder and also includes a second system logic device having a dynamic bus inversion decoder. The first and second system logic devices are coupled via a data bus. The encoder compares a group of data bits currently placed on the data bus with a next group of data bits to be placed on the data bus. If the encoder determines that greater than a predetermined number of bit transitions would occur between the current and next group of data bits, the encoder inverts the next group of data bits before placing the next group of data bits onto the data bus. The encoder also asserts an inversion signal that is received by the decoder. In response to the assertion of the inversion signal, the decoder inverts the previously inverted next group of data bits to restore the original data.

WO 02/39290 A2

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METHOD AND APPARATUS FOR REDUCING SIMULTANEOUS SWITCHING OUTPUT NOISE USING DYNAMIC BUS INVERSION

Field Of The Invention

The present invention pertains to the field of computer systems. More particularly, this invention pertains to the field of reducing simultaneous switching output noise on a data bus.

Background of the Invention

In an effort to increase performance in today's computer systems, system designers seek to increase clock frequencies on various system data busses. As bus frequencies increase, noise on the data lines becomes an increasingly important issue. An increase in clock frequency, and its corresponding reduction in clock period, allows for less time for noise present on data lines to settle before data is latched at the receiving end. Noise present on data lines at the time data is latched at the receiving end may result in the latching of invalid data.

One source of noise on data lines may be referred to as simultaneous switching output noise. This noise results from several to many output drivers on a particular device switching states at the same time. One example of this may include a system logic device driving 32 bits of data at once to a graphics device over a graphics bus. The system logic device may drive 32 bits of "1"s during one clock period and then drive 32 bits of "0"s during the next clock period. In this example all of the graphics bus bits change state from one clock period to the next. Such transitions may induce simultaneous switching output noise on some or all of the 32 data lines and limit the possible clock frequency for the graphics bus, thereby limiting the potential performance of the graphics subsystem.

Brief Description of the Drawings

The invention will be understood more fully from the detailed description given below and from the accompanying drawings of embodiments of the invention which, however, should not be taken to limit the invention to the specific embodiments described, but are for explanation and understanding only.

Figure 1 is a block diagram of an embodiment of a system including a system logic device having a dynamic bus inversion encoder and a graphics device having a dynamic bus inversion decoder.

Figure 2 is a block diagram of an embodiment of a dynamic bus inversion encoder.

Figure 3 is a flow diagram of an embodiment of a method for reducing simultaneous switching output noise using dynamic bus inversion.

Detailed Description

Figure 1 is a block diagram of an embodiment of a system 100 including a system logic device 120 having a dynamic bus inversion (DBI) encoder 200 and a graphics device 130 having a DBI decoder 124. The system 100 also includes a processor 110 coupled to the system logic device 120. The system logic device is further coupled to a system memory 140 and an input/output hub 150.

The system logic device 120 is coupled to the graphics device 130 by way of an output data bus 203 and an inversion signal 205. The DBI encoder 200 compares a set of data bits previously placed on the output data bus 203 with a next set of data bits to be placed on the data bus 203. The DBI encoder 200 determines how many data bit transitions would occur on the data bus 203 as a result of the next set of data bits being driven on the data bus 203 following the previous set of data bits. If the number of potential data bit transitions is greater than a predetermined number, then the DBI encoder 200 inverts each data bit in the next set of data bits and drives the inverted data onto the output data bus 203. The DBI encoder 200 asserts the inversion signal 205 to indicate to

the DBI decoder 124 that the data bits have been inverted. The DBI decoder 124 then inverts the inverted data bits in order to restore the original data.

The predetermined number is selected to produce the fewest bit transitions. For some embodiments, the predetermined number is selected to equal one half of the data width. For example, for a group of 16 bits of data, the predetermined number would be 8. Therefore, if more than 8 data bits would change state, the data bits are inverted and the inversion signal is asserted.

The DBI embodiment described above reduces the amount of simultaneous switching output noise by limiting the number of bit transitions occurring on the output data bus.

An embodiment of the decoder 124 includes an XOR circuit that performs an XOR function on the incoming data and the inversion signal. In this manner, if no inversion is indicated (the inversion signal 205 is a "0") then the incoming data is not inverted by the decoder 124. If an inversion is indicated (the inversion signal 205 is a "1") then each bit of incoming data is inverted by the decoder 124 in order to restore the original data.

Although system 100 shows a single data bus and a single inversion signal, the data bus 203 may be divided into two or more groups. For example, a 32 bit bus may be divided into two groups of 16 bits each. Other configurations are possible. Inversion decisions are then made by the encoder 200 on a group-by-group basis. Each group utilizes its own inversion signal.

Figure 2 is a block diagram of an embodiment of the dynamic bus inversion encoder 200. Data to be delivered over the output data bus 203 is delivered to the encoder 200 via an internal data bus 201. For this embodiment, the internal data bus 201 and the output data bus 203 are 16 bits wide. Other embodiments are possible with a data width of 32 bits organized into two groups of 16 bits each. Still other embodiments are possible with other data organizations and groupings.

The internal data 201 is delivered to both an XOR circuit 210 and an inverter 220/multiplexor 230 combination. The XOR circuit 210 also receives output data 203.

The output data 203 represents a current set of data bits. An XOR operation is performed on the input data 201 and the output data 203. An inversion determination circuit 240 receives the output of the XOR operation and determines whether the number of data bit transitions found by the XOR operation exceeds a predetermined number. For this example embodiment, the predetermined number is eight. Other embodiments are possible using other predetermined numbers. It is also possible to implement the encoder 200 using a programmable predetermined number. If the inversion determination circuit 240 determines that the number of data bit transitions exceeds the predetermined number, an internal inversion signal 209 is asserted.

The internal inversion signal 209 is delivered to the multiplexor 230 and a latch 260. If the internal inversion signal 209 is asserted, indicating that the predetermined number of data bit transitions is exceeded, then the multiplexor 230 delivers the output of the inverter circuit 220 to a latch 250. If the internal inversion signal is not asserted, then the multiplexor 230 delivers the non-inverted internal data to the latch 250. The latch 250 then latches the output of the multiplexor 230 onto the output data bus 203. The internal inversion signal 209 is latched onto the inversion signal 205.

The inverter 220/multiplexor 230 combination may be implemented as an XOR circuit where the internal data bus bits 201 are each XORed with the internal inversion signal 209. When the internal inversion signal 209 is asserted, then each of the internal data bits 201 are inverted and delivered to the input of the latch 250. If the internal inversion signal 209 is not asserted, then the XOR operation will leave the internal data bits 201 unchanged.

Figure 3 is a flow diagram of an embodiment of a method for reducing simultaneous switching output noise using dynamic bus inversion. At block 310, a first n bits of data are delivered over a data bus. The number of bit transitions between the first n bits of data and a second n bits of data are counted at block 320. As indicated at block 330, if the counted bit transitions exceeds a predetermined number, then the next n bits of data are inverted at block 340. The inverted next n bits of data are delivered over the data

bus at block 360. An inversion signal is also asserted at block 360. If the counted bit transitions do not exceed the predetermined number, then the next n bits of data are delivered over the data bus at block 350. The preceding embodiment of a method may be repeated for every subsequent n bits of data to be delivered over the data bus. For this embodiment, n equals 16 and the predetermined number is eight, although other embodiments are possible using other data widths and predetermined numbers.

Although some of the previously discussed embodiments mention a system logic device transmitting data to a graphics device over a graphics bus, other embodiments are possible using any system device as a transmitter having a DBI encoder and using any other device as a receiver having a DBI decoder.

In the foregoing specification the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than in a restrictive sense.

Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments, of the invention. The various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments.

CLAIMS

What is claimed is:

1. An apparatus, comprising:

a bit transition detection circuit to determine whether a next bus transaction would result in greater than a predetermined number of bit transitions when compared with a current bus transaction, the bit transition detection circuit to assert an inversion signal if the next bus transaction would result in greater than the predetermined number of bit transitions when compared with the current bus transaction; and

an inversion circuit to invert the bits of the next bus transaction in response to an assertion of the inversion signal.

2. The apparatus of claim 1, wherein the bit detection circuit includes a first XOR circuit to sense a number of bit transitions between the current bus transaction and the next bus transaction.

3. The apparatus of claim 2, wherein the bit detection circuitry includes a circuit to determine whether the number of bit transitions sensed by the first XOR circuit exceeds the predetermined number.

4. The apparatus of claim 3, wherein the inversion circuit includes a second XOR circuit to perform an XOR function between the next bus transaction and the inversion signal.

5. The apparatus of claim 4, further comprising a first latch to latch the output of the second XOR circuit, the first latch to provide the latched output to an external data bus and further to provide the latched output to the first XOR circuit.

6. The apparatus of claim 5, further comprising a second latch to latch the inversion signal and to provide the latched inversion signal to an external inversion signal.

7. The apparatus of claim 6, wherein the current and next bus transactions are sixteen bits wide.

8. The apparatus of claim 7, wherein the predetermined number of bit transitions is eight.

9. A method, comprising:

determining whether a next bus transaction would result in greater than a predetermined number of bit transactions when compared with a current bus transaction; and

providing an inverted version of the next bus transaction.

10. The method of claim 9, further comprising providing an inversion signal to indicate that the next bus transaction is inverted.

11. A method, comprising:

delivering a first n bits of data over a data bus;

counting bit transitions between the first n bits of data and a second n bits of data;

determining whether the counted bit transitions exceed a predetermined number;

inverting the next n bits of data and asserting an inversion signal if the counted bit transitions exceed the predetermined number; and

delivering the next n bits over the data bus.

12. The method of claim 11, wherein inverting the next n bits includes performing an XOR operation between the next n bits and the inversion signal.

13. The method of claim 12, wherein n is sixteen.

14. The method of claim 13, wherein the predetermined number is eight.

15. A system, comprising:

a processor;

a first logic device coupled to the processor, the system logic device including a dynamic bus inversion encoder, the dynamic bus inversion encoder including

a bit transition detection circuit to determine whether a next bus transaction would result in greater than a predetermined number of bit transitions when compared with a current bus transaction, the bit transition detection circuit to assert an inversion signal if the

next bus transaction would result in greater than the predetermined number of bit transitions when compared with the current bus transaction, and

an inversion circuit to invert the bits of the next bus transaction in response to an assertion of the inversion signal; and

a second logic device coupled to the first logic device via a bus.

16. The system of claim 15, wherein the bit detection circuit includes a first XOR circuit to sense a number of bit transitions between the current bus transaction and the next bus transaction.

17. The system of claim 16, wherein the bit detection circuitry includes a circuit to determine whether the number of bit transitions sensed by the first XOR circuit exceeds the predetermined number.

18. The system of claim 17, wherein the inversion circuit includes a second XOR circuit to perform an XOR function between the next bus transaction and the inversion signal.

19. The system of claim 17, further comprising a first latch to latch the output of the second XOR circuit, the first latch to provide the latched output to the bus and further to provide the latched output to the first XOR circuit.

20. The system of claim 19, further comprising a second latch to latch the inversion signal and to provide the latched inversion signal to an external inversion signal, the external inversion signal coupled to the second logic device.

21. The system of claim 20, wherein the second logic device includes a dynamic bus inversion decoder.

21. An apparatus, comprising:

a data bus input to receive n bits of data;

an inversion signal input to receive an inversion signal; and

an inversion circuit to invert the n bits of data received at the data bus input if the inversion signal is asserted.

22. The apparatus of claim 21, wherein the inversion circuit includes an XOR circuit to perform an XOR function between the n bits of data received at the data bus input and the inversion signal.

23. The apparatus of claim 22 wherein n is 16.

24. A method, comprising:

receiving n bits of data at a receiving device; and

inverting the n bits of data in response to an assertion of an inversion signal, the inversion signal asserted by a transmitting device.

25. The method of claim 24, wherein inverting the n bits of data includes performing an XOR function between the n bits of data and the inversion signal.

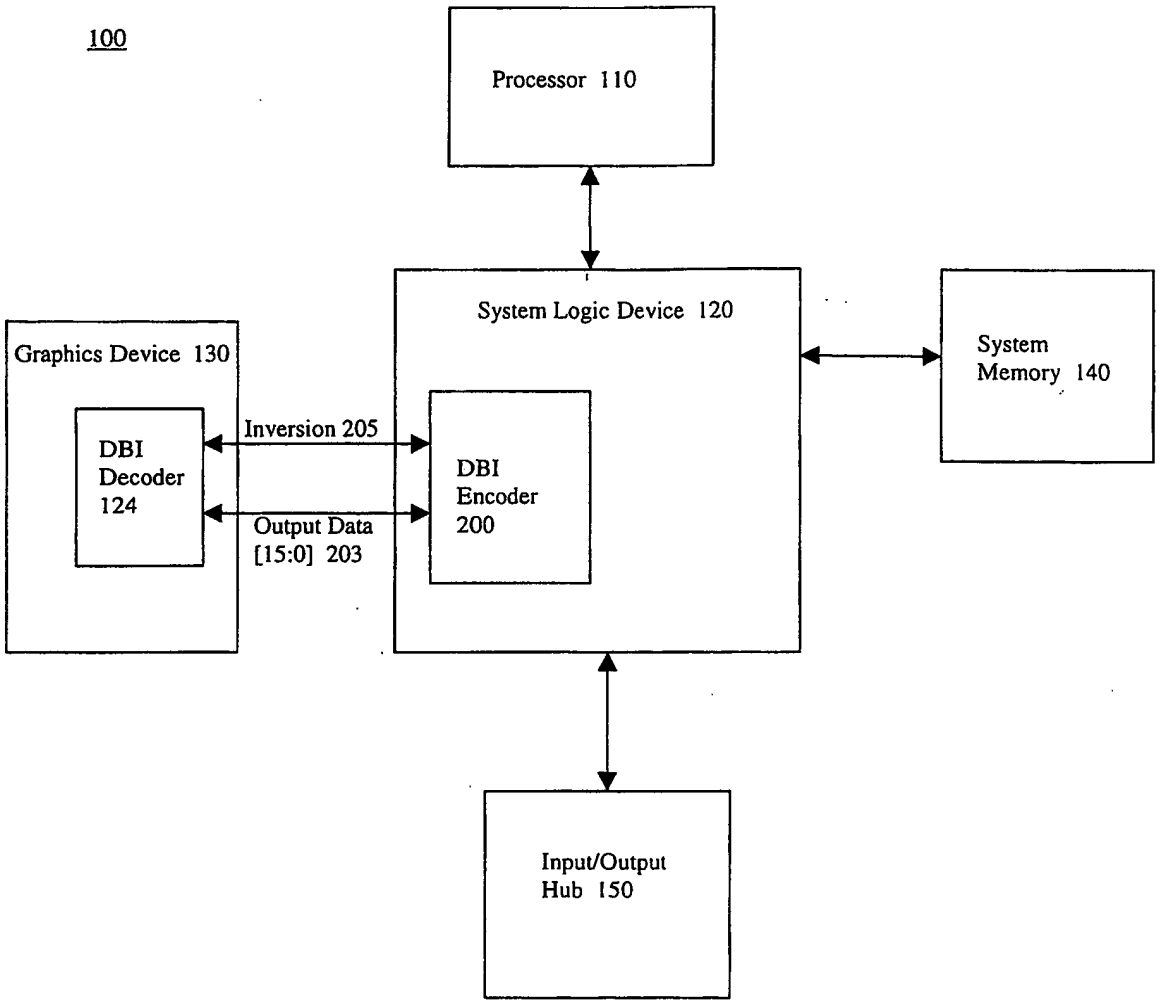
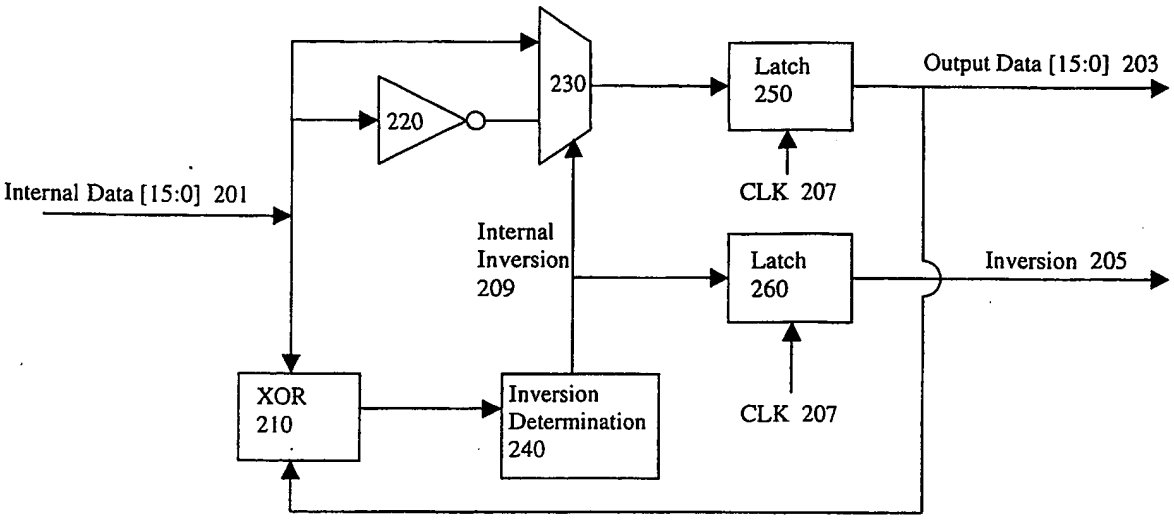

100
Processor 110
System Logic Device 120
Graphics Device 130
DBI Decoder 124
Inversion 205
Output Data [15:0] 203
DBI Encoder 200
System Memory 140
Input/Output Hub 150

Figure 1

200


230
220
Latch
250
Output Data [15:0] 203
Internal Data [15:0] 201
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Internal
Inversion
209
Latch
260
Inversion 205
XOR
210
Inversion
Determination
240
CLK 207

Figure 2

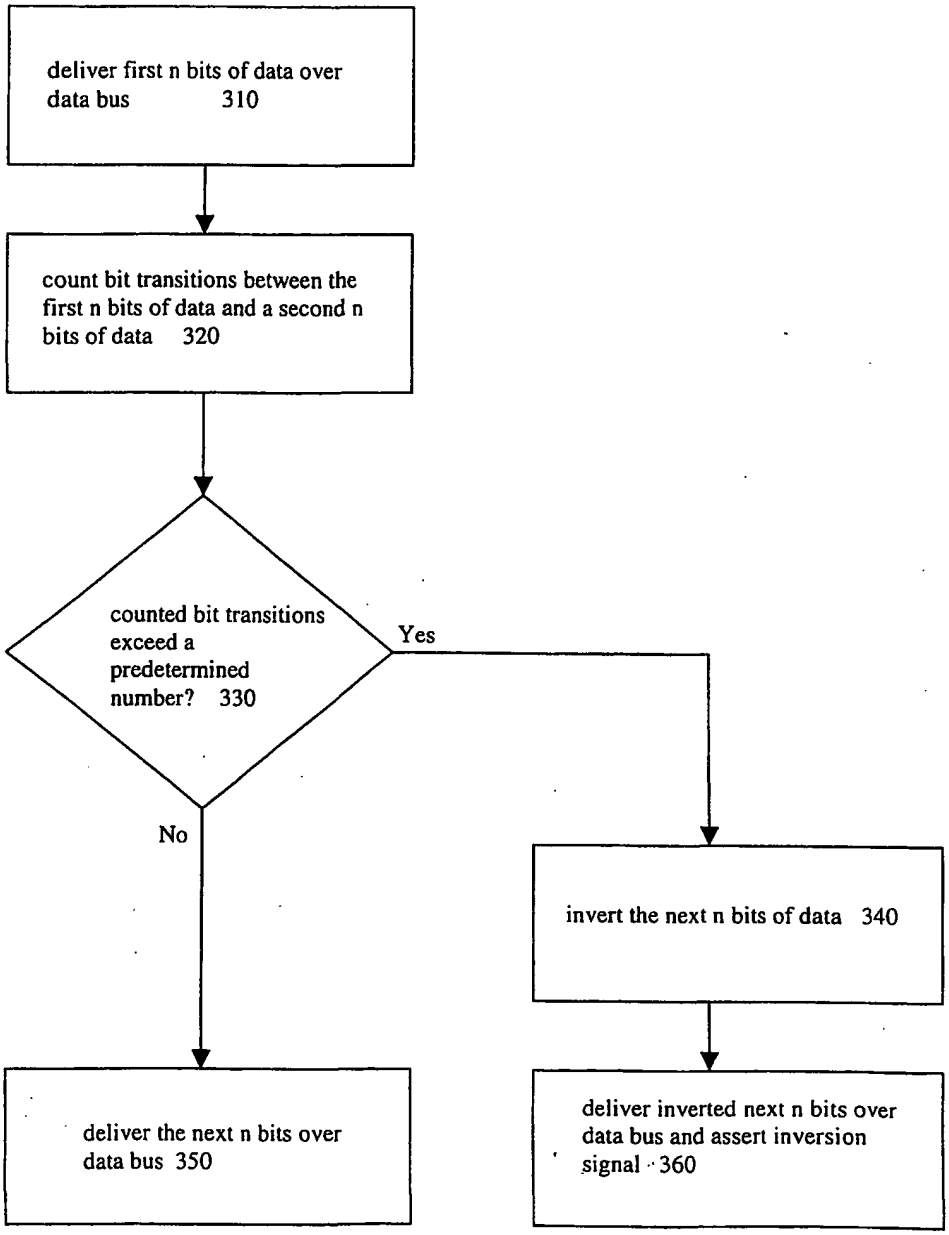
deliver first n bits of data over data bus 310
count bit transitions between the first n bits of data and a second n bits of data 320
counted bit transitions exceed a predetermined number? 330
Yes
No
invert the next n bits of data 340
deliver the next n bits over data bus 350
deliver inverted next n bits over data bus and assert inversion signal 360

Figure 3